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Project 1

Phase 2

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The goal of Project 1 Phase 2 was to continue finishing the datapath of the mini-RISC processor. Adding the controller and logic in the ALU. The datapath receives 3 bits for the ALU operations and 6 other control bits.

The ALU operations are as follows: 001 for addition, 010 for and, 011 for or, 100 for xor, 101 for logical shift, 110 for arithmetic shift, and 111 for load immediate into upper.

The functions of the 6 control bits are as follows: C1 decides whether to take the sign extended immediate value or the value from the Rsrc register, C2 decides whether to take the 1’s complement of the value coming in, C3 is for carry in for subtraction, C4 decides whether to take 0 or the value from the Rdest register, C5 decides whether to write to the register file and C6 decides whether data memory is accessed.

The dm, rf, and pm modules take a pointer to an int array as a parameter. When these modules are instantiated, the parameter is used to load the modules with an initial value. In order to test whether these modules instantiated correctly, a simple test bench instantiated the modules and checked if the values at certain addresses where correct. An initial array of {0, 4, 5, 6} was used and the results are as follows.

The modules are correctly initialized and verified. The datapath takes the submodules of rf, dm, pm, and alu and instantiates them in its constructor. The main program takes the controller and connects it to the datapath. The result is shown below.

The main program instantiates and finishes with no errors.